1. An integrated circuit module comprising:

at least one known good integrated circuit die having multiple selectable input functions, multiple selectable output functions, common functions, a function selector, all interconnected and connected to input/output pads;

a second level substrate onto which the known good integrated circuit die is mounted having connections to the input/output pads of the known good integrated circuit die to select desired selectable input functions and output functions and provide signal paths to transfer signals to the desired selectable input function and signals from the desired selectable input function and signals to and from the common functions, wiring connections between the connections to the input/output pads and external circuitry whereby appropriate logic states are applied to input/output pads connected to the function selector to select the desired selectable input functions and desired selectable input functions to configure a functional operation of said integrated circuit module; and

pins connected to the second level substrate to provide physical and electrical connections between the external circuitry and the wiring connections on the second level substrate.

2. The integrated circuit module of claim 1 wherein the known good die is a DRAM having a plurality of selectable input/output organizations, whereby each of the selectable input/output organizations is selected as one of the logic states to the output function selector and connections from the second level substrate to unused output function connected to input/output pads of the DRAM are omitted from the second level substrate.

3. The integrated circuit module of claim 1 wherein the known good die is a computational processor.

4. The integrated circuit module of claim 3 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

5. The integrated circuit module of claim 1 wherein the input/output pads of the known good integrated circuit die are created during processing of a semiconductor wafer one to which the known good integrated circuit die is formed.

6. The integrated circuit of claim 1 wherein the input/output pads are gang-bonded to the second level substrate.

7. The integrated circuit of claim 1 wherein the known good integrated circuit die is attached to the second level substrate by a flip chip assembly.

8. The integrated circuit module of claim 1 wherein the input/output pads of the known good die have solder bumps and are arranged as a ball grid array.

9. The integrated circuit module of claim 1 wherein the second level substrate is selected from the group of substrates consisting of plastic substrates, fiberglass reinforced plastic substrates, ceramic substrates, insulator coated metal substrate, semiconductor integrated circuit die, and glass substrates.

10. The integrated circuit of claim 1 wherein in the second level substrate is a known good integrated circuit die of a second type on to which the known good integrated circuit die is mounted, whereby said known good integrated circuit die of the second type has multiple selectable input functions, multiple selectable output functions, common functions, a function selector, all interconnected and connected to input/output pads.

11. The integrated circuit of claim 10 wherein the known good integrated circuit die is a DRAM and the known good integrated circuit die of the second type is a computational processor.

12. The integrated circuit module of claim 11 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

13. A DRAM integrated circuit module comprising:

at least one known good DRAM die having address input pads connected to address selection circuitry, timing and control input pads connected to timing and control circuitry, an array of DRAM cells to retain digital data connected to the address selection circuitry and time and control circuitry, a plurality of input/output buffers connected to inputs and outputs of the array of DRAM cells to transfer digital data to and from said array of DRAM cells, a plurality of data transfer pads connected to input/output buffers, an option selector circuit connected to the input/output buffers to select which of the plurality of data transfer pads are to contain the digital data for transfer to and

from the array of DRAM cells, and a plurality of option select pads connected to the option selector circuit to provide appropriate logic states to the option selector circuit to select the data transfer pads;

a DRAM module substrate onto which the known good DRAM die is mounted having wiring connections between the address input pads, timing and control pads, the selected data transfer pads, the option select pads, and external circuitry; and

a plurality of pins mounted to the module substrate to connect the wiring connections to the external circuitry.

14. The DRAM module of claim 13 wherein the address input pads, timing and control pads, data transfer pads, and option select pads are arranged in a ball grid array, whereby non-selected data transfer pins and appropriate option select pads are omitted from connection to the DRAM module substrate.

15. A digital processor module comprising:

at least one known good computational processor die having a plurality of memory data transfer pads arranged in groups of memory data buses, a plurality of memory address transfer pads arranged in groups of memory address buses, a plurality of input/output interface data transfer pads arranged in

input/output interfaces, and a plurality of timing and control transfer pads arranged in timing and control interfaces, all connected to a computational processor to manipulate digital data transferred into said computational processor and transfer digital data from said computational processor, and a bus configurator connected to the memory data transfer pads, the memory address transfer pads, the input/output interface pads, and the timing and control transfer pads to configure the memory data buses, the memory address buses, the input/output interfaces, and the timing and control interfaces for transfer and manipulation of digital data, whereby the bus configurator is connected to bus configuration pads to provide logic states to determine the bus configuration;

a digital processor module substrate onto which the known good processor die is mounted having connections between external circuitry and the configured memory data buses, memory address buses, the input/output interface buses, and the timing and control interface bus; and

a plurality of pins mounted to the module substrate to connect the connections to the external circuitry.

16. The digital processor module of claim 15 wherein the memory data transfer pads, the memory address transfer pads, the input/output

interface data transfer pads, and the timing and control transfer pads are arranged in a ball grid array.

17. The digital processor module of claim 15 wherein the non-selected memory data transfer pads, memory address transfer pads, the input/output interface data transfer pads, timing and control transfer pads, and bus configuration pads are omitted from connection to the digital processor module.

18. The digital processor module of claim 15 wherein the memory data transfer pads, the memory address transfer pads, the input/output interface data transfer pads, timing and control transfer pads have solder bumps.

19. An integrated circuit module comprising:

at least one known good integrated circuit die of a first type having multiple selectable input functions, multiple selectable output functions, common functions, a function selector, all interconnected and connected to input/output pads;

at least one known good integrated circuit die of a second type having multiple selectable input functions, multiple selectable

output functions, common functions, a function selector, all interconnected and connected to input/output pads;

a second level substrate onto which the known good integrated circuit dies of the first and second type are mounted having connections to the input/output pads of the known good integrated circuit dies of the first and second type to select desired selectable input functions and output functions and provide signal paths to transfer signals to the desired selectable input function and signals from the desired selectable input function and signals to and from the common functions, wiring connections between the connections to the input/output pads and external circuitry whereby appropriate logic states are applied to input/output pads connected to the function selector to select the desired selectable input functions and desired selectable input functions to configure a functional operation of said integrated circuit module; and

pins connected to the second level substrate to provide physical and electrical connections between the external circuitry and the wiring connections on the second level substrate.

20. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the first type is a DRAM having a plurality of selectable input/output organizations, whereby each of the selectable input/output organizations is selected as one of the logic states to the output function selector and connections from the second level substrate to unused output function connected to input/output pads of the DRAM are omitted from the second level substrate.

21. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the second type is a computational processor.

22. The integrated circuit module of claim 21 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

23. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the second type is a DRAM having a plurality of selectable input/output organizations, whereby each of the selectable input/output organizations is selected as one of the logic states to the output function selector and connections from the second level substrate to unused output function connected to input/output pads of the DRAM are omitted from the second level substrate.

24. The integrated circuit module of claim 19 wherein the known good integrated circuit die of the first type is a computational processor.

25. The integrated circuit module of claim 23 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

26. The integrated circuit module of claim 19 wherein the input/output pads of the known good integrated circuit dies of the first and second types are created during processing of a semiconductor wafer one to which the known good integrated circuit die is formed.

27. The integrated circuit of claim 19 wherein the input/output pads are gang-bonded to the second level substrate.

28. The integrated circuit of claim 19 wherein the known good integrated circuit dies of the first and second types are attached to the second level substrate by a flip chip assembly.

testing said integrated circuit die to functional integrated circuits die,

dicing said semiconductor wafer to circuit die, and

sorting said known good integrated circuit die; and

forming a second level substrate by the steps of:

forming metal interconnections on all levels of the second level substrate, and laminating of the levels of the second level substrate, and

applying a solder mask to a component level of said second level substrate in locations to expose the input/output pads of the common functions, desired functions of the multiple selectable input functions and the multiple selectable output functions, and the input/output pads to select the desired functions with input and output selector functions;

applying a solder paste to the input/output pads exposed by the solder mask,

placing and securing the known good integrated circuit die to said component level; and

performing final assembly and test of said integrated circuit module.

32. The method of claim 31 further comprising applying solder bumps to the input/output pads.

29. The integrated circuit module of claim 19 wherein the input/output pads of the known good integrated circuit dies of the first and second types have solder bumps and are arranged as a ball grid array.

30. The integrated circuit module of claim 19 wherein the second level substrate is selected from the group of substrates consisting of plastic substrates, fiberglass reinforced plastic substrates, ceramic substrates, insulator coated metal substrate, semiconductor substrate, glass substrates, and an integrated circuit die forming a chip-on-chip structure.

31. A method to form an integrated circuit module comprising the steps of:

forming a known good integrated circuit die having multiple selectable input functions, multiple selectable output functions, common functions, a selector function by the steps of;

forming electronic components on a surface of a semiconductor wafer to form the multiple selectable input functions, the multiple selectable output functions, common functions, and the selector function,

forming redistribution metallurgy on the surface of the semiconductor wafer to form input/output pads connected to the multiple selectable input functions, the multiple selectable output functions, the common functions, and the selector functions,

33. The method of claim 31 further comprising, subsequent to dicing said semiconductor substrate, burning in said functional integrated circuit die.

34. The method of claim 31 further comprising testing of functional integrated circuit die subsequent to dicing to determine said known good integrated circuit die.

35. The method of claim 31 further comprising arranging the input/output pads as a ball grid array.

36. The method of claim 31 wherein the known good integrated circuit die is selected from a group of integrated circuit dies consisting of DRAM dies, digital signal processor dies, microcontroller dies, microprocessor dies, and digital logic arrays.

37. The method of claim 31 further comprising omitting non-desired functions of the multiple selectable input functions, the multiple selectable output functions, the input selector function and output selector function by omitting coating of the input/output pads of said non-desired functions with the solder paste.

38. An input/output integrated circuit connection system to physically and electrically secure a known good integrated circuit die to a second level substrate, whereby the known good integrated circuit die has multiple selectable input functions, multiple selectable output functions, multiple common functions, input function selectors and output function selectors, whereby said input/output integrated circuit connection system comprises:

a plurality of input/output pads formed as a redistribution metal layer on a top surface of said known good integrated circuit die and arranged in rows and columns to form an array; and

a plurality of solder balls placed on the input/output pads; and

a solder mask placed on a component surface of the second level substrate, having voids to allow connections of the solder balls of the input/output pads of the common functions, and desired multiple selectable input functions, desired multiple selectable output functions, desired connections of the input function selector, and desired connections of the output function selector to wiring contacts on the second level substrate, and no voids to prevent connection of the solder balls of undesired function and undesired connections to the input and output function selectors.

39. The input/output integrated circuit connection system of claim 38 wherein the wiring contacts on the second level substrate are connected to external circuitry.

40. The input/output integrated circuit connection system of claim 38 wherein the second level substrate is selected from the group of substrates consisting of plastic substrates, fiberglass reinforced plastic substrates, ceramic substrates, insulator coated metal substrate, semiconductor substrates, glass substrates, and integrated circuit substrates to for a chip-on-chip structure.

41. The input/output integrated circuit connection system of claim 38 wherein the known good integrated circuit die is a DRAM and the multiple selectable input and output functions are the number of bits to be transferred into and out of said DRAM.

42. The input/output integrated circuit connection system of claim 38 wherein the known good integrated circuit die is a computational processor.

43. The integrated circuit module of claim 42 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

44. The input/output integrated circuit connection system of claim 38 wherein the desired connections and the undesired connections of the function selector create logic states at the inputs of said function selector to choose the desired input functions and the desired output functions.

45. A method to form integrated circuit connections to physically and electrically connect a known good integrated circuit die to a second level substrate, whereby the known good integrated circuit die comprises multiple selectable input functions, multiple selectable output functions, multiple function selectors, and whereby said method comprises the steps of:

forming a plurality of input/output pads of a redistribution metal on a top surface of said known good integrated circuit die;

arranging said input/output pads in rows and columns

forming solder bumps on said input/output pads;

placing a solder mask on a component surface of the second level substrate, having voids to allow connections of the solder balls of the input/output pads of the common functions, and desired multiple selectable input functions, desired multiple selectable output functions, desired connections of the function selector to wiring contacts on the second level substrate, and no voids to

prevent connection of the solder balls of undesired function and undesired connections to the function selectors; and

melting said solder bumps to make connections between said known good integrated circuit die and signal path within said second level substrate.

46. The method of claim 45 wherein said wiring paths on the second level substrate interconnect the known good integrated circuit die with external circuitry.

47. The method of claim 45 wherein the second level substrate is selected from the group of substrates consisting of plastic substrates, fiberglass reinforced plastic substrates, ceramic substrates, insulator coated metal substrate, semiconductor substrates, glass substrates, and an integrated circuit die to form a chip-on-chip structure.

48. The method of claim 45 wherein the known good integrated circuit die is a DRAM and the multiple selectable input and output functions are the number of bits to be transferred into and out of said DRAM.

49. The method of claim 45 wherein the known good integrated circuit die is a computational processor.

50. The integrated circuit module of claim 49 wherein the computational processor is a selected from the set of computational processors consisting of microprocessors, microcontroller, and digital signal processors.

51. The method of claim 45 wherein the desired connections and the undesired connections of the function selector create logic states at the inputs of said function selector to choose the desired input functions and the desired output functions.